CPS 590- Lab 1  
 Mahamudul Islam(500963051)

**Question 1.**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Memory** | |  | **CPU registers** | | |
|  |  |  |  |  |  |
| 300 | 3705 |  |  | 300 | PC |
|  |  |  |  |  |  |
| 301 | 5305 |  | 0000 | | AC |
| 302 |  |  |  |  | IR |
| 7706 |  |  | 3705 |
|  |  |  |  |  |  |
| 303 | 0000 |  |  |  |  |
|  |  |  | | |  |
| 304 | 0000 |  | 0003 | | Device 5 |
|  |  |  |  | |  |
| 305 | 0002 |  | 0000 | | Device 6 |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Memory** | |  | **CPU registers** | | |
|  |  |  |  |  |  |
| 300 | 3705 |  |  | 301 | PC |
|  |  |  |  |  |  |
| 301 | 5305 |  | 0003 | | AC |
| 302 |  |  |  |  | IR |
| 7706 |  |  | 3705 |
|  |  |  |  |  |  |
| 303 | 0000 |  |  |  |  |
|  |  |  | | |  |
| 304 | 0000 |  | 0003 | | Device 5 |
|  |  |  |  | |  |
| 305 | 0002 |  | 0000 | | Device 6 |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

**Fetch Stage (1) Execute Stage (1)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Memory** | |  | **CPU registers** | | |
|  |  |  |  |  |  |
| 300 | 3705 |  |  | 301 | PC |
|  |  |  |  |  |  |
| 301 | 5305 |  | 0003 | | AC |
| 302 |  |  |  |  | IR |
| 7706 |  |  | 5305 |
|  |  |  |  |  |  |
| 303 | 0000 |  |  |  |  |
|  |  |  | | |  |
| 304 | 0000 |  | 0003 | | Device 5 |
|  |  |  |  | |  |
| 305 | 0002 |  | 0000 | | Device 6 |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Memory** | |  | **CPU registers** | | |
|  |  |  |  |  |  |
| 300 | 3705 |  |  | 302 | PC |
|  |  |  |  |  |  |
| 301 | 5305 |  | 0005 | | AC |
| 302 |  |  |  |  | IR |
| 7706 |  |  | 5305 |
|  |  |  |  |  |  |
| 303 | 0000 |  |  |  |  |
|  |  |  | | |  |
| 304 | 0000 |  | 0003 | | Device 5 |
|  |  |  |  | |  |
| 305 | 0002 |  | 0000 | | Device 6 |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

**Fetch Stage (2) Execute Stage(2)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Memory** | |  | **CPU registers** | | |
|  |  |  |  |  |  |
| 300 | 3705 |  |  | 303 | PC |
|  |  |  |  |  |  |
| 301 | 5305 |  | 0005 | | AC |
| 302 |  |  |  |  | IR |
| 7706 |  |  | 7706 |
|  |  |  |  |  |  |
| 303 | 0000 |  |  |  |  |
|  |  |  | | |  |
| 304 | 0000 |  | 0003 | | Device 5 |
|  |  |  |  | |  |
| 305 | 0002 |  | 0005 | | Device 6 |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

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| --- | --- | --- | --- | --- | --- |
| **Memory** | |  | **CPU registers** | | |
|  |  |  |  |  |  |
| 300 | 3705 |  |  | 302 | PC |
|  |  |  |  |  |  |
| 301 | 5305 |  | 0003 | | AC |
| 302 |  |  |  |  | IR |
| 7706 |  |  | 7706 |
|  |  |  |  |  |  |
| 303 | 0000 |  |  |  |  |
|  |  |  | | |  |
| 304 | 0000 |  | 0003 | | Device 5 |
|  |  |  |  | |  |
| 305 | 0002 |  | 0000 | | Device 6 |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

**Fetch Stage (3)** **Execute Stage(3)**

**Question 2.**

A.

Here I1 starts at t=10 as it has the lowest time and it ends at t=40 as it requires 30-time units.

Then I2 starts at t=40 and it ends at t=50 because of the 10-time units required time.

Finally, I3 starts at t=50 and ends at t=100 as it requires 50-time units.

B.

For I1 the interrupt time is t=10 so it starts after t=10 and with the time required is 30 but after 20 time units when t=30 I3 is started because I3 has the highest priority so I3 ends at t=80 as it require 50 time units. Then it returns to I1 again and restarts it and runs it for 10 more-time units and I1 ends at t=90.  
At last I2 is started at t=90 and finishes at t=100 as it requires only 10-time units.

**Question 3.**

On average it will take 1.0 µt

As we know,  
  
Avg time = H \* T1 + (1 - H) \* (T2 + T1)

1.0 = H\*0.5+(1-H)\*(1.0+0.5)  
1.0 = 0.5H+(1-H)\*1.5

1.0=0.5H+1.5-1.5H

1.0-1.5 = -1.0H

-0.5 = -1.0H

H= 0.5  
So the hit ratio should be H ≥ 0.5 to be better off with just level 2 memory.